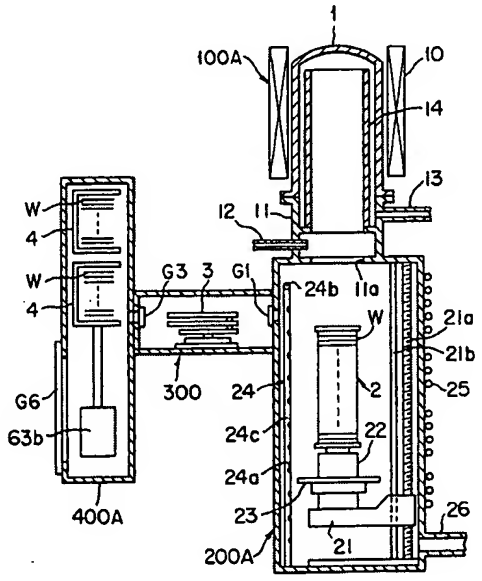
Remarks

Claims 1–12 are pending in this application. Claims 1 and 7 are independent; Claims 2–6 depend from Claim 1, and Claims 8–12 depend from Claim 7. Claims 1–12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,388,944 ("Takanabe"). Claims 1 and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,709,521 ("Hiroki").

Claim Rejections Under § 102(b) based on Takanabe.

Claims 1–12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Takanabe. By its own terms, Takanabe discloses a semiconductor processing apparatus that includes a heat-treatment section 100A, a load lock chamber 200A, a robot chamber 300, and a cassette chamber 400A. On the other hand, the Examiner has characterized 100A/200A as a reaction chamber, 300 as a transfer chamber, and 400A as a load lock chamber. Regardless of the nomenclature, once a semiconductor wafer W is transferred to chamber 100A/200A, it is transferred to wafer boat 2, which supports the wafer W during processing. This structure is illustrated in Figure 3 of Takanabe, which is reproduced below.



In contrast to the disclosure of Takanabe, Applicants have amended Claim 1 to recite:

> Claim 1 (currently amended): Vacuum load lock semiconductor wafer processing equipment, comprising:
> a load lock chamber,
> a transfer chamber,
> a reaction chamber located above said transfer chamber, and
> a robot located outside said load lock chamber that includes a wafer transfer arm **that is configured to support said semiconductor wafers in the reaction chamber during a wafer processing process**,
> wherein said wafer transfer arm is adapted to operate inside said load lock chamber and inside a vacuum, and is adapted to transfer said semiconductor wafers between the load lock chamber, the transfer chamber, and the reaction chamber. [*emphasis added*]

Takanabe does not anticipate this claim. In the Takanabe apparatus, the wafer boat 2 supports the wafer W during processing. The wafer boat 2 is not analogous to the "wafer transfer arm" recited in Claim 1 because it is not "adapted to transfer said semiconductor wafers between the load lock chamber, the transfer chamber, and the reaction chamber".

In view of the foregoing, Applicants submit that Takanabe does not anticipate Claim 1, and therefore respectfully suggest that Claim 1 is allowable over Takanabe. Furthermore, because Claims 2–6 depend from Claim 1, Applicants submit that Claims 2–6 are allowable over Takanabe for the same reasons that Claim 1 is allowable over Takanabe, in addition to reciting further distinguishing features of particular utility.

Likewise, Applicants have amended Claim 7 to recite:

> Claim 7 (currently amended): A method of processing semiconductor wafers, comprising:
> providing a load lock chamber, a transfer chamber, and a reaction chamber, wherein said reaction chamber is located above said transfer chamber,
> providing a robot that includes a wafer transfer arm, wherein said wafer transfer arm is adapted to operate inside said load lock chamber and inside a vacuum **and to support said semiconductor wafers in the reaction chamber during a wafer processing process**, and
> transferring said semiconductor wafers between said load lock chamber, said transfer chamber, and said reaction chamber using said wafer transfer arm. [*emphasis added*]

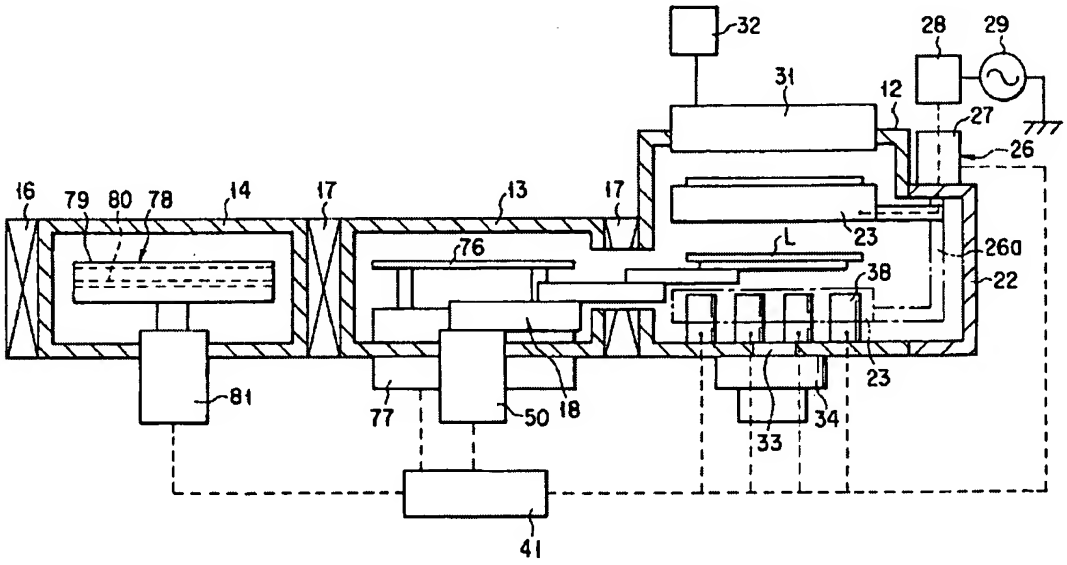
Takanabe does not anticipate this claim. As described above, in the Takanabe apparatus, the wafer boat 2 supports the wafer W during processing. The wafer boat 2 is not analogous to the "wafer transfer arm" recited in Claim 7 because it is not used to

transfer "said semiconductor wafers between said load lock chamber, said transfer chamber, and said reaction chamber".

In view of the foregoing, Applicants submit that Takanabe does not anticipate Claim 7, and therefore respectfully suggest that Claim 7 is allowable over Takanabe. Furthermore, because Claims 8–12 depend from Claim 7, Applicants submit that Claims 8–12 are allowable over Takanabe for the same reasons that Claim 7 is allowable over Takanabe, in addition to reciting further distinguishing features of particular utility.

Claim Rejections Under § 102(e) based on Hiroki.

Claims 1 and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hiroki. Hiroki discloses a semiconductor processing system that includes a load lock chamber 14, a transfer chamber 13, and a process chamber 12. A transfer apparatus 18 is provided in the transfer chamber 13, and is configured to load an LCD substrate L from the load lock chamber 14 to the process chamber 12, and vice versa. In the process chamber 12, the transfer apparatus 18 is configured to place the LCD substrate L onto a worktable 23, which supports the LCD substrate during processing. This structure is illustrated in Figure 2 of Hiroki, which is reproduced below.



In contrast to the disclosure of Hiroki, Applicants have amended Claim 1 to recite:

> Claim 1 (currently amended): Vacuum load lock semiconductor wafer processing equipment, comprising:
> a load lock chamber,
> a transfer chamber,
> a reaction chamber located above said transfer chamber, and
> a robot located outside said load lock chamber that includes a wafer transfer arm **that is configured to support said semiconductor wafers in the reaction chamber during a wafer processing process,**
> wherein said wafer transfer arm is adapted to operate inside said load lock chamber and inside a vacuum, and is adapted to transfer said semiconductor wafers between the load lock chamber, the transfer chamber, and the reaction chamber. [*emphasis added*]

Hiroki does not anticipate this claim. In the Hiroki apparatus, the worktable 23 supports the LCD substrate L during processing. The worktable 23 is not analogous to the "wafer transfer arm" recited in Claim 1 because it is not "adapted to transfer said semiconductor wafers between the load lock chamber, the transfer chamber, and the reaction chamber". Therefore, Applicants submit that Hiroki does not anticipate Claim 1, and thus respectfully suggest that Claim 1 is allowable over Hiroki.

Likewise, Applicants have amended Claim 7 to recite:

> Claim 7 (currently amended): A method of processing semiconductor wafers, comprising:
> providing a load lock chamber, a transfer chamber, and a reaction chamber, wherein said reaction chamber is located above said transfer chamber,
> providing a robot that includes a wafer transfer arm, wherein said wafer transfer arm is adapted to operate inside said load lock chamber and inside a vacuum **and to support said semiconductor wafers in the reaction chamber during a wafer processing process**, and
> transferring said semiconductor wafers between said load lock chamber, said transfer chamber, and said reaction chamber using said wafer transfer arm. [*emphasis added*]

Hiroki does not anticipate this claim. As described above, in the Hiroki apparatus, the worktable 23 supports the LCD substrate L during processing. The worktable 23 is not analogous to the "wafer transfer arm" recited in Claim 7 because it is not used to transfer "said semiconductor wafers between said load lock chamber, said transfer chamber, and said reaction chamber". Therefore, Applicants submit that Hiroki does not anticipate Claim 7, and thus respectfully suggest that Claim 7 is allowable over Hiroki.

New Claims.

Applicants have added new Claims 13–22. Claims 13 and 17 are independent; Claims 14–16 depend from Claim 13, and Claims 18–22 depend from Claim 17. Claim 13 recites, among other limitations, "a transfer chamber exhaust port configured to exhaust gases within the transfer chamber and the reaction chamber from a position lower than a wafer processing position." Similarly, Claim 17 recites, among other limitations, "removing gases from the transfer chamber and the reaction chamber through a transfer chamber exhaust port that is positioned below a wafer processing position." These new claims are supported by Figure 3 of the originally filed disclosure, which illustrates transfer chamber exhaust port 26 positioned below the semiconductor wafer 40. Applicants note that in Takanabe, robot chamber 300—and not the reaction chamber—is evacuated through gate valves G1 and G2, which are not positioned below the semiconductor wafer (see Takanabe, Figure 3).

Applicants have also added new Claims 23–30. Claims 23 and 27 are independent; Claims 24–26 depend from Claim 23, and Claims 28–30 depend from Claim 27. Claim 23 recites, among other limitations, a wafer transfer arm "that is configured to support the wafer in the reaction chamber during a wafer processing operation." Similarly, Claim 27 recites, among other limitations, that "the semiconductor wafer is supported in the reaction chamber by the wafer transfer arm during a wafer processing operation." These new claims are supported by Figure 2 of the originally filed disclosure, which illustrates the semiconductor wafer 40 supported by the wafer transfer arm during a wafer processing operation. As noted above with respect to independent Claims 1 and 7, neither Takanabe nor Hiroki disclose a wafer transfer arm that is configured to support a wafer during a wafer processing operation.

Conclusion.

In view of the foregoing amendments, Applicants submit that this application is in condition for allowance, and respectfully request the same. If, however, some issue remains that the Examiner feels can be addressed by an Examiner's Amendment, the Examiner is cordially invited to call the undersigned for authorization.

Respectfully submitted,

KNOBBE MARTENS OLSON & BEAR LLP

Dated: 6 aug 04

By: Kyle Schlueter

Kyle F. Schlueter
Registration No. 54,912
Attorney of Record
Customer No. 20,995
(310) 551-3450

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